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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,930	09/19/2003	Warren M. Farnworth	2269-5529US (02-0766.00/U	6453

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/666,930	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 25-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 25-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 8/31/05. Currently, claims 1-14 and 25-39 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 9/06/05 was filed after the mailing date of the Office Action on 5/27/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 recites the limitation "including forming the ring of material only from the material of the semiconductor wafer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 lacks antecedent basis in independent claim 1, lines 7-8, that includes the limitation "leaving a ring of material comprising at least in part a material of the semiconductor wafer along the periphery thereof;" Specifically, this limitation requires that the ring of material includes at least a portion of the semiconductor wafer. However in claim 3, the ring of material is required to have only the material of the semiconductor wafer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 25 is rejected under 35 U.S.C. 102(b) as being anticipated by Lu US Patent 5,827,394.

Lu discloses the semiconductor method as claimed. See figures 1-6 and corresponding text, where Lu teaches a method for processing a semiconductor wafer comprising: mounting an adhesive-coated tape **30** to a surface of a semiconductor wafer **32a-c** (figure 3; col. 6, lines 60-67); and singulating individual components from the semiconductor wafer and removing at least some singulated individual components without using a film frame while the adhesive-coated tape is mounted to the surface thereof (figures 4-6; col. 11, lines 1-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-14 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu US Patent 5,827,394 in view of McKenna et al., US Patent 6,471,806.

Lu discloses the semiconductor method substantially as claimed. See figures 1-6 and corresponding text, where Lu shows, pertaining to claim 1, a method for supporting wafers for singulation and pick-and-place, comprising: providing a semiconductor wafer **32a-c** (figure 3; col. 6, lines 60-67; col. 7, lines 1-5); mounting an adhesive-coated tape **30** to a surface of the semiconductor wafer (figure 3; col. 7, lines 5-18); singulating individual components from the semiconductor wafer, leaving a ring of material comprising in part a material of the semiconductor wafer along the periphery thereof (figure 3; col. 6, lines 60-67); and removing at least some individual components from the adhesive-coated tape (figures 4-6; col. 11, lines 1-45) . In addition, Lu shows, pertaining to claim 3, further including forming the ring of material only from the material of the semiconductor wafer (figure 3; col. 6, lines 60-67). Also, Lu shows, pertaining to claim 4, further including forming at least a portion of the ring of material from a polymer material disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer (figure 3; col. 7, lines 5-20). Lu shows, pertaining to claim 5, further including forming the ring of material in part from the material of the semiconductor wafer and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer (figure 3; col. 7, lines 1-20). In addition, Lu shows, pertaining to claim 6, further comprising forming the ring of material from the polymer material by one of spin-coating, sterolithography or molding (figure 3; col. 6, lines 1-51) . Lu shows, pertaining to claim 8, further comprising mounting the adhesive-coated tape to an active surface of the semiconductor wafer and singulating the semiconductor wafer from the backside thereof after backgrinding (figure 3; col. 6, lines 60-67). In addition, Lu shows, pertaining to claim 9,

further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof (figure 3; col. 6, lines 60-67). Also, Lu shows, pertaining to claim 10, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor from an active surface thereof (figure 3; col. 6, lines 60-67). Lu shows, pertaining to claim 11, wherein mounting the adhesive-coated tape comprises mounting a tape bearing a UV-sensitive adhesive thereon (figure 3; col. 3, lines 60-67). In addition, Lu shows, pertaining to claim 12, further comprising exposing the UV-sensitive adhesive prior to removing the at least some individual components while leaving a portion on the adhesive-coated tape extending over the ring of material unexposed (figure 4; col. 9, lines 27-51). Also, Lu shows, pertaining to claim 13, wherein the semiconductor wafer is singulated using one of laser cutting, water cutting and sawing (figure 3; col. 6, lines 60-67). Finally, Lu shows, pertaining to claim 14, further comprising discarding the ring of material, any remaining individual components and the adhesive-coated tape after removing the at least some individual components (figure 6; col. 11, lines 1-15, ***Note***: the Examiner takes the position that since Lu teaches conventional pick and place processing method, the discarding of the ring of material and any remaining individual components would result in routine manufacturing processing).

Lu shows, pertaining to claim 29, a method of processing a semiconductor wafer, comprising: singulating individual components from the semiconductor wafer while leaving an uncut peripheral ring of material of material comprising at least in part a material of the semiconductor wafer thereabout (figure 3; col. 6, lines 60-67; col. 7, lines 1-15). In addition, Lu shows, pertaining to claim 30, further including removing at least some singulated individual

components therefrom (figure 6; col. 11, lines 5-10). Also, Lu shows, pertaining to claim 32, further comprising defining the uncut peripheral ring of material from semiconductor material (figure 3; col. 6, lines 60-67; col. 7, lines 1-5). Lu shows, pertaining to claim 33, further comprising defining the uncut peripheral ring of material at least in part from a polymer disposed about and contiguous with the semiconductor wafer (figure 3; col. 6, lines 60-67). Finally, Lu shows, pertaining to claim 34, further comprising defining the uncut peripheral ring of material in part form semiconductor material and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer (figure 3; col. 6, lines 60-67).

However, Lu fails to show, pertaining to claims 1 and 29, gripping the semiconductor wafer along at least a portion of a periphery thereof. In addition, Lu fails to show, pertaining to claims 2 and 31, wherein gripping the semiconductor wafer along at least a portion of the periphery there of further includes gripping the semiconductor wafer by the ring of material during the removing of the at least some individual components.

McKenna teaches, in figures 1-5, and corresponding text a similar method for supporting wafers for singulation where the semiconductor wafer is gripped at the periphery thereof by a vacuum pressure applied to the perimeter of the wafer (col. 4, lines 42-51).

It would have been obvious to one of ordinary skill in the art, to substitute the following steps of: gripping the semiconductor wafer along at least a portion of a periphery thereof; wherein gripping the semiconductor wafer along at least a portion of the periphery there of further includes gripping the semiconductor wafer by the ring of material during the removing of the at least some individual components, in the method of Lu, pertaining to claims 1, 2, 29 and 31, according to the teachings of McKenna, with the motivation that, by gripping the periphery

of semiconductor wafer, the semiconductor wafer will be securely mounted to the adhesive tape, resulting in a more efficient mounting technique for later manufacturing processes such as pick and place methods.

Claims 7 and 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu US Patent 5,827,394 in view of McKenna et al., US Patent 6,471,806 in further view of Oka US Patent 6,551,906.

Lu in view of McKenna discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-6, 8-14 and 29-34 are rejected under 35 U.S.C. 103(a)

However, Lu in view of McKenna fails to show, pertaining to claim 7, further comprising backgrinding the semiconductor wafer prior to singulation. In addition, Lu in view of McKenna fails to show pertaining to claim 35, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle a 200 mm semiconductor wafer saw chuck. Also, Lu in view of McKenna fails to show, pertaining to claim 36, further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck. Lu in view of McKenna fails to show, pertaining to claim 37, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom. In addition, Lu in view of McKenna fails to show, pertaining to claim 38, a method of using a 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers. Finally, Lu in view of McKenna fails to show, pertaining to claim 39,

further including processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps: wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle a 200 mm semiconductor wafer saw chuck; further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom; a method of using a 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers; further including processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers, in the method of Lu, pertaining to claims 7 and 35-39, according to the teachings of Oka, with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to

accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu US Patent 5,827,394 in view of Oka US Patent 6,551,906.

Lu discloses the semiconductor method substantially as claimed. See preceding rejection of claim 25 under 35 U.S.C. 102(b).

However, Lu fails to show, pertaining to claim 26, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. In addition, Tandy fails to show, pertaining to claim 27 further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck. Finally, Tandy fails to show, pertaining to claim 28, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singluated individual components therefrom.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps: wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers; further including singulating the 300 mm semiconductor wafer using a

200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom, in the method of Lu, pertaining to claims 26-28, according to the teachings of Oka, with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Response to Arguments

Applicant's arguments with respect to claims 1-14, 25-28-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

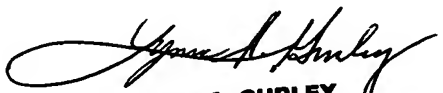
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Stanetta Isaac
Patent Examiner
November 10, 2005